MODEL PROBLEM SET

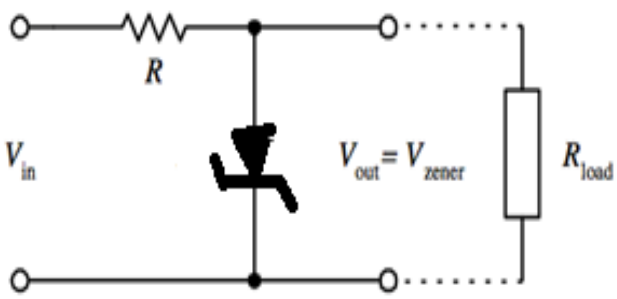
Analog Systems and Application (UPC: 32221403)

B.Sc. (H) Physics IV Sem

PARA I and II

1. A 220V, 50 Hz ac is applied to the primary of 5:1 step up transformer with centre tapped secondary. This rectifier has a resistive load of 1 kΩ. Calculate,
(a) DC power to the load
(b) Power rating of Secondary
(c)Ripple factor
(d) Peak Inverse Voltage (PIV) across each diode

2. **(a)** For the given circuit diagram of zener diode, the input voltage (V_i)= 120 volts, series resistance (R_i)= 5 kΩ, Load resistance (R_L) = 10 kΩ and zener voltage (V_z)= 50 volts. Find the current flowing through the zener diode. **[Ans: 9 mA]**



(b) For the same circuit of a zener diode, R_s =30 Ω, V_z =18 V and R_L = 200 Ω. If the input voltage (V_i) can vary from 20 V to 30 V. Find
(i) The minimum and maximum current in the diode
(ii) The minimum and maximum power dissipated in the diode
(iii) The minimum and maximum power dissipated in the series resistance R_s.

3. A sample of Ge is doped to the extent of 10^{14} donor atoms/cm^3 and 7 x 10^{13} acceptor atoms/cm^3. At room temperature, the resistivity of pure Ge is 60 O-cm. If the applied electric field is 2 V /cm, find total conduction current density. **[Ans: 52.3 mA/cm^3]**

4. Over what range of input voltage will the zener regulator circuit maintains 30V across 2 kΩ resistor, assuming R_s = 200 Ω and max. zener current is 25 mA

5. A diode whose internal resistance is 20 Ω is to supply power to a 1000Ω load from a 110 V (rms) source of supply. Calculate (a) The peak load current. (b) The DC load current (e) AC Load Current (d) The DC diode voltage. (e) The total input power to the circuit. (f) % regulation from no load to the given load.
[Ans: 152.5 mA, 48.5 mA, 76.2 mA, -48.5 V, 5.9 W, 2.05 %]

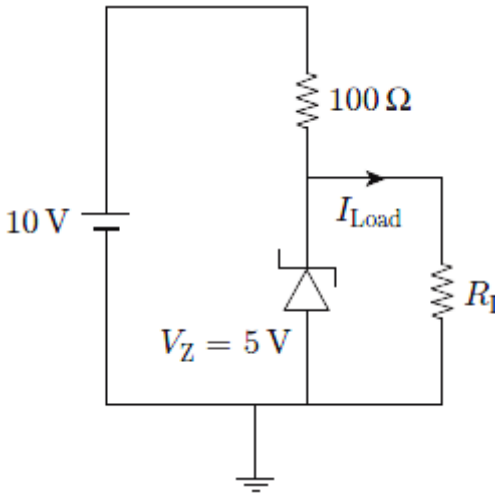
6. A 1 mA meter whose resistance is 10 Ω is calibrated to read rms volts when used in a bridge circuit with semiconductor diodes. The effective resistance of each element may be considered to be zero in the forward direction and infinity in the reverse direction. The sinusoidal input voltage is applied in series with a 5 - KOhm resistance. What is the full scale reading of this meter?

7. A half wave rectifier allows current to flow from time $t1 = \pi/6\omega$ to $t2 = 5\pi/6\omega$, the A.C. Voltage being given by Vs = 100 Sin ωt. Calculate the RMS and DC output voltage.
[Ans: 5.56 V, 17.38 V]

8. A full wave rectifier circuit with C-type capacitor filter is to supply a D.C. Current of 20 mA at16V. If frequency is 50 Hz ripple allowed is 5% Calculate:

(a) *Required secondary voltage of the transformer.* **[Ans: 38 V]**
(b) *Ratio of I peak/I max through diodes.* **[Ans: 2]**
(c) *The value of* C *required.* **[Ans: 72 µF]**

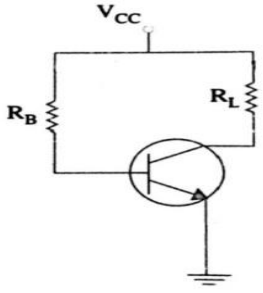
9. In the following circuit, the knee current of the ideal Zener diode is 10 mA. To maintain 5 V across R_L, find the minimum value of R_L in Ω. and the minimum power rating of the Zener diode in mW.



10. An abrupt p-n junction of Ge (dielectric constant=16) has resistivity of 3 Ω-cm on p-side and of 1 Ω-cm on n-side. Calculate (a) Barrier Potential (b) Width of depletion region. Given, n_i = 1.5 x 10^{13} cm^{-3}, μ_n= 4000 $cm^2 V^{-1} sec^{-1}$, μ_p= 2000$cm^2 V^{-1} sec^{-1}$&$\frac{kT}{q}$= 0.026 V.
[Ans: N_A= 1.04 x 10^{15} cm^{-3}, N_D= 1.56 x 10^{15} cm^{-3}, V_0 = 0.23 V, W=0.8 µm.]
11. Calculate the avalanche breakdown voltage of a Ge p-n step junction diode in which N_D >> N_A and N_A= $10^{21}/m^3$ and the critical field strength is 2 x 10^7 V/m. The dielectric constant of Ge, $\varepsilon_r$is 16. **[Ans: 177 V]**
12. A Zener diode is to be designed to have a breakdown voltage of 500V. Assume that avalanche breakdown occurs at a field intensity of 10^7 V/m. If the donor density, N_D is 10^{23} m^{-3}, what acceptor density N_A should be used? The relative dielectric constant for the material (semiconductor) is 11.5 and permittivity of free space is 8.85 x 10^{-12} F/m.
[Ans: N_A= 6.3 x 10^{19} m^{-3}]
13. In an n-type Si crystal (band gap= 1.1 eV), it is desirable to have the fermi level 0.10 eV below the bottom of the CB. The intrinsic carrier concentration n_i = 1.5 x 10^{10} cm^{-3}. Find the donor concentration. Assume equal effective masses for electron and hole.
[Ans: N_D= 10^{18} cm^{-3}]

PARA III and IV

1. A change of 8mA in the emitter current causes one of the 7.9 mA in the collector current. Calculate the values of α and β. **[Ans: α=0.9875, β=79]**
2. In the CB configuration of a transistor, the current amplification factor is 0.95. Calculate the base current when the emitter current is 2 mA. **[Ans: 0.1 mA]**
3. A transistor with current gain equal to 0.975 and a reverse saturation current I_{CO} of 10 µA is operated in the CE configuration as shown in figure below. If the base current is 250 µA, calculate the emitter and collector currents. **[Ans: I_E= 20 mA, I_C = 19.8 mA]**

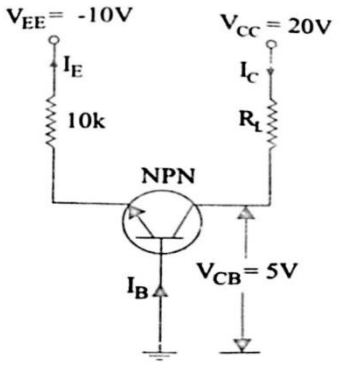


4. Discuss the operation of a PNP transistor. The reverse saturation current in a PNP germanium transistor is 8 µA. If the transistor common base current gain is 0.979, calculate the collector and emitter current for 40 µA base current. What is the collector current when base current is zero?
[Ans: I_E= 1.94 mA, I_C = 1.9 mA]

5. A CE transistor amplifier is driven by a voltage source V_s of internal resistance R_s of 800 Ω. The load impedance R_L is 2000Ω. The parameters are h_{fe} = 50, h_{ie} = 1100Ω, h_{re} = 2.5×10^4, h_{oe} = 25 μAV^{-1}.Calculate the performance quantities.

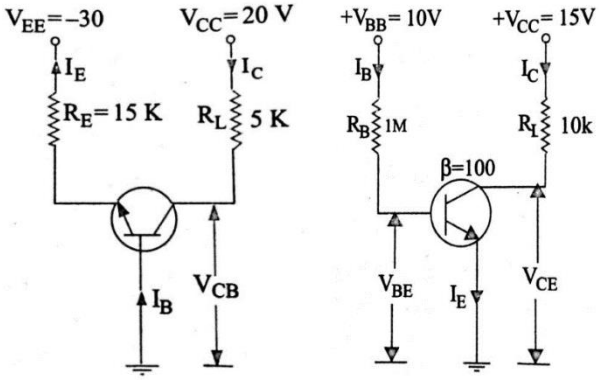
[Ans: A_i= -47.6, Z_i =1076 Ω, A_v= -88.47, Z_o =54.28 kΩ, A_p= 4211]

6. In the circuit given below, what value of R_L causes V_{CB} = 5V? **[Ans: 15 kΩ]**



7. For the circuit given below, find (i) I_B (ii) I_C (iii) I_E and (iv) V_{CE}. Neglect V_{BE}.

[Ans: 10 μA, 1 mA, 1.01 mA, 5V]



8. For the circuit shown above, a) draw the dc load line and b) locate its quiescent or dc working points. **[Ans: (b) (10 V, 2 mA)]**

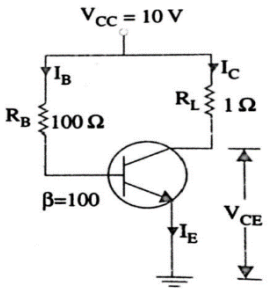
9. An amplifier has an input signal of 16V peak to peak and an input impedance of 320KΩ. It gives an output voltage of 8V peak to peak across a load resistor of 4Ω. Calculate the dB power gain of the amplifier. **[Ans: 43 dB]**

10. A certain radio receiver delivers an output power of 3.6W.

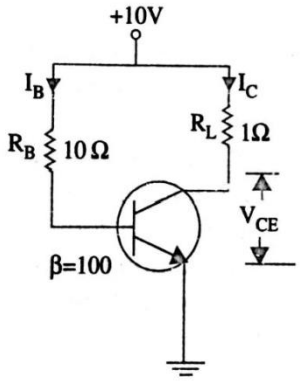
i) What would be the decibel gain if power output is increased to 7.2W? **[Ans: 3 dB]**

ii) What power output would be required to produce a power gain of 10dB? **[A: 36 W]**

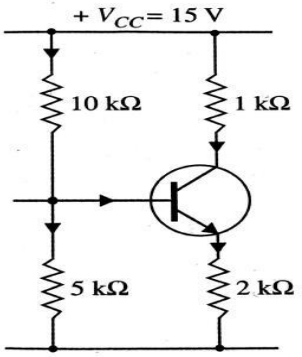
11. For the CE circuit given below, find the values of V_{CE}. Take β = 100 and neglect V_{BE}. Is the transistor working in cut-off or saturation? **[Ans: Saturation]**



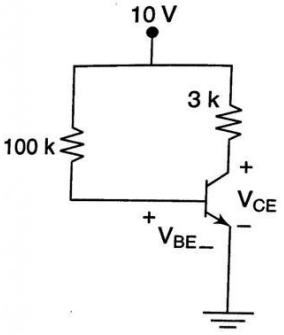
12. Find out whether the transistor of below figure is working in saturation or well into saturation. Neglect VBE. **[Ans: Well into Saturation]**



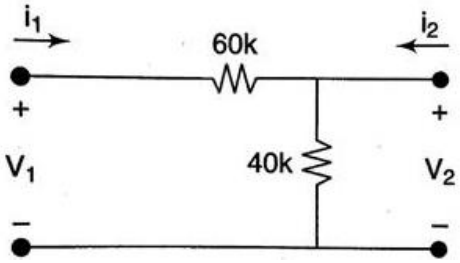
13. Figure given below shows the voltage divider bias method. Draw the dc load line and determine the operating point. Assume the transistor to be of silicon. **[Ans: 8.55V, 2.15 mA)]**



14. What should be the minimum value of current gain β of the transistor (See figure) so that the transistor operates in the saturation region, where the other parameters are: $V_{BE(sat)}$= 0.8 V , $V_{CE(sat)}$= 0.2 V. **[Ans: 36]**

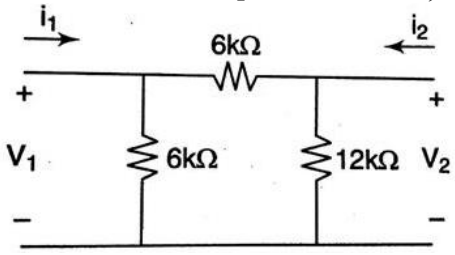


15. Find the h-parameters for the network shown below: -
[Ans: h_i=60 kΩ, h_r=1, h_f=-1, h_o=25 μs]



16. Determine the h-parameters for the following network: -

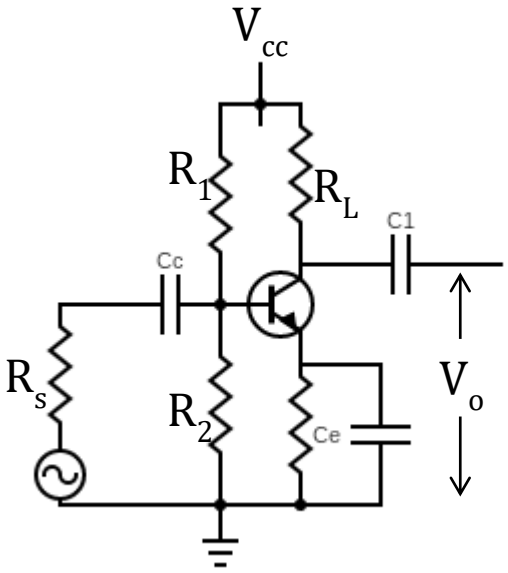
[Ans: h_i=3 kΩ, h_r=1/2, h_f=-1/2, h_o=1/6 ms]



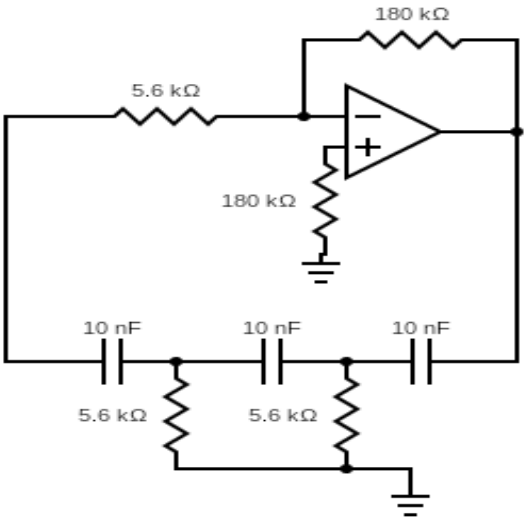
PARA V, VI and VII

Coupled amplifiers, feedback in amplifiers, sinusoidal oscillators

1. There amplifier stages are working in cascade with 0.05V peak to peak input providing 150 V peak to peak output. If the voltage gain of the first stage is 20 and input to the third stage is 15 V peak to peak, determine
   (i) The overall voltage gain **[Ans: 3000]**
   (ii) Voltage gain of 2nd and 3rd stages. **[Ans: 15, 10]**
   (iii) Input voltage of the 2nd stage. **[Ans: 1 V_{pp}]**
2. Calculate the size of coupling capacitor C_c to provide a low frequency 3dB point at 100Hz if R_s=600 Ω, h_{ie}=1K Ω, h_{fe}=50, R_1=5.2K Ω, R_2=1.24K Ω. Assume
   (i) An ideal bypass capacitor R_c=0 Ω **[Ans: 1.45 µF]**
   (ii) A practical bypass capacitor R_c=15 Ω. **[Ans: 1.26 µF]**



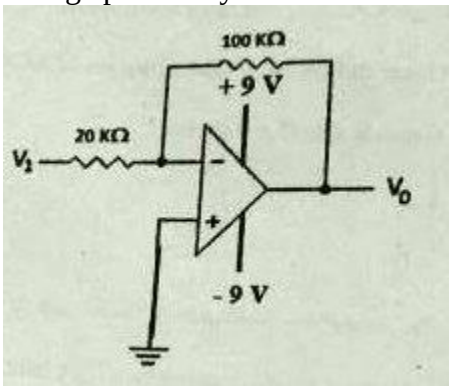
3. Calculate the size of bypass capacitor C_e to provide a low frequency 3 dB point of 100 Hz when R_e=1K Ω, h_{fe} =50, h_{ie}=1K Ω and R_s=600 Ω. Determine the input and output impedance with feedback for voltage series feedback having A=-100, R_i=10 K Ω, R_o=20 K Ω for feedback of (i) β=-0.1 (ii) β=-0.5.
   [Ans: C_e=50 µF, (i) Z_{if}=110kΩ, Z_{of}=1.82 kΩ, (ii) Z_{if}=510kΩ, Z_{of}=392.16 Ω]
4. Using a 741 OPAMP with a ±10V supply, design a phase shift oscillator to produce a 1 KHz output frequency.



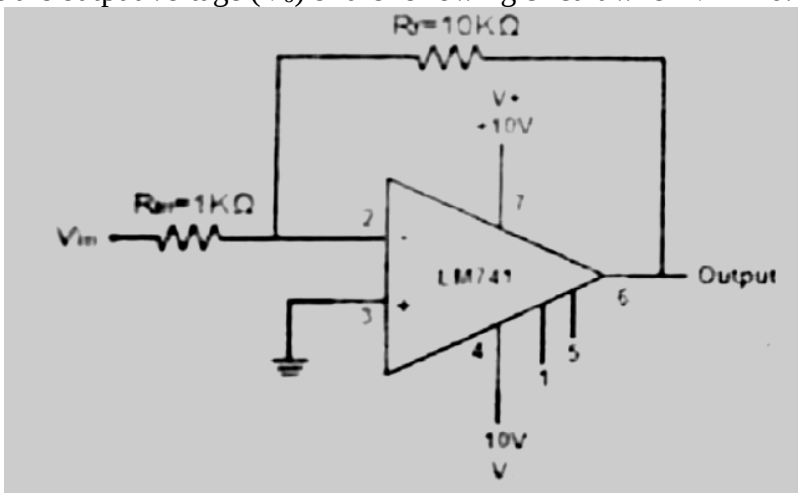
5. Design a BJT phase shift oscillator to produce a 900 Hz output with a 10 V peak to peak amplitude. Assume that the BJT has h_{fe} (min) ≈60 and hie≈1.5K Ω.
6. Analyse the BJT Hartley oscillator to determine the oscillating frequency. The important component values are L_1=L_2=4.7mH, C_1=600 pF, C_2=C_3=0.03μF. the mutual inductance between L_1 and L_2 is 100 μH. **[Ans: 66.3 kHz]**
7. An amplifier with a 1K Ω input resistance and a 50 K Ω output resistance has a voltage gain. The amplifier is now modified to provide a 10% negative voltage feedback in series with the input. Calculate
   (i) The voltage gain with feedback **[Ans: 8]**
   (ii) The input resistance with feedback **[Ans: 5 kΩ]**
   (iii) The output resistance with feedback. **[Ans: 10 kΩ]**
8. An engineer designs an amplifier to have a voltage gain of 60, but when constructed it only has a gain of 50. A technician suggests that positive feedback could be used to increase the gain to the required level. Then, (a) How much feedback should be used to provide the desired level? (b) What value of feedback will double the gain? (c) What disadvantage may arise from this type of feedback? (d) What percentage of feedback will cause oscillations? **[Ans: (a) 0.33%, (b) 1%, (d) 2%]**
9. A feedback network (to be used with an amplifier to provide oscillations) is tested and found to give an output of 0.0125 V with a 0.5 V input (a) What must be the minimum gain of the amplifier to provide oscillations? (b) What will be the effect on the output if the amplifier's gain is twice that required by the Barkhausen criterion? (c) What percentage of negative feedback should be introduced to the amplifier so that linear oscillations result? **[Ans: (a) 40, (b) Non-linear Osc., (c) -1.25%]**
10. A three section RC phase shift oscillator has R=10 KΩ and C=0.001 μF. (a) What is the frequency of oscillations? (b) If the oscillator is to be made variable using the same value of R, what should be the tuning range of the capacitors to obtain a frequency range of 1 to 100 KHz? **[Ans: (a) 6.5 kHz, (b) 65 pF to 0.0065 μF]**
11. A Colpitt's oscillator used as the local oscillator in an AM radio receiver to produce frequencies from 1 to 2 MHz (a) what must be the inductance of the coil if the minimum capacitance obtainable is 43 pF (C_1 and C_2)? (b) What must be the maximum value of C to produce the necessary frequencies? (c) What frequencies would be produced if this coil were used in a Hartley oscillator circuit with C=100 pF?
12. An amplifier gives output of 5V at distortions of 10% with 2mV input signal. Distortions are to be restricted to only 1% using feedback. How much should be the input signal to get an output of 5V? **[Ans: 20 mV]**

PARA VIII, IX and X

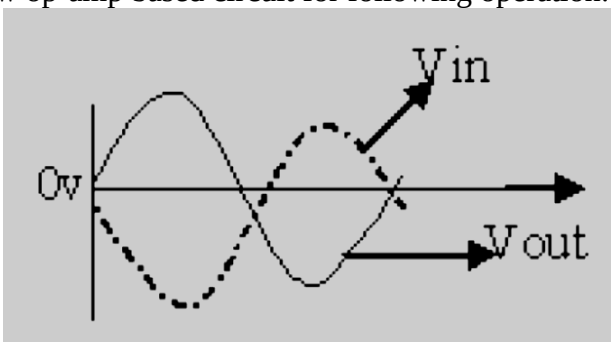
1. Draw the circuit of a non-inverting amplifier of gain 11 using an op-amp.
2. Design an op-amp circuit with gain -20. Assume input resistance is 5 kΩ.
3. Determine the output voltage of the following circuit when V_1 = 1V, 5V and sin (ωt). Also show the output voltage pictorially in last case. **[Ans: -5V, -8V, -5sin(ωt)]**



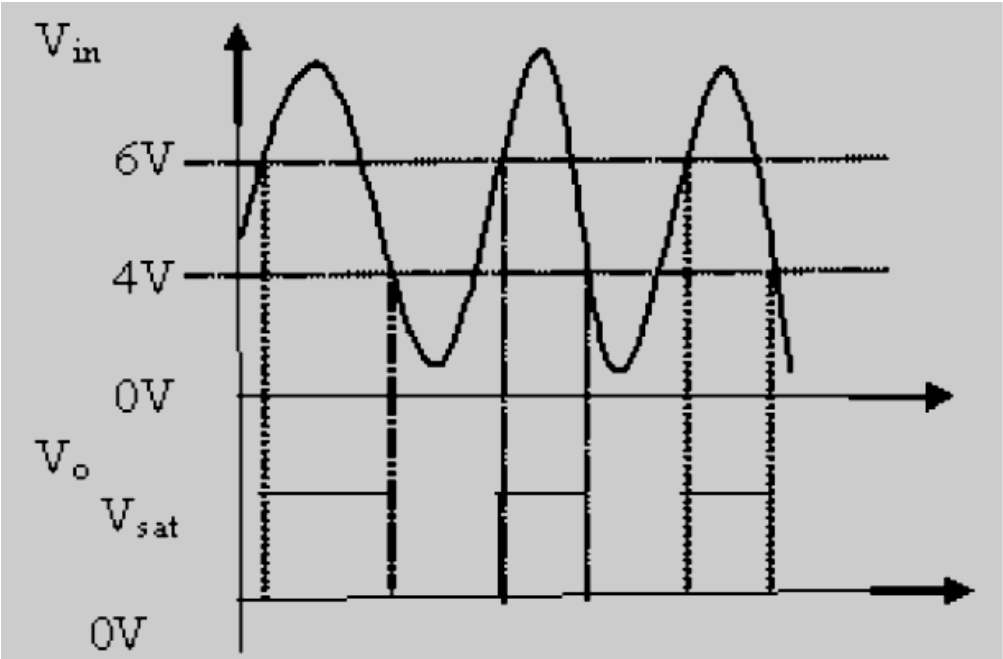
4. What would be the output of an op-amp in the inverting mode if the input resistance is 1 kΩ and feedback resistance is (a) 2 kΩ and (b) 20 kΩ for a dc input signal of 1.5 V? (V_{sat} = ± 14V) **[Ans: (a) -3V, (b) -14V]**
5. Estimate the output voltage (V_o) of the following circuit when Vin = 0.2 V. **[Ans: -2V]**



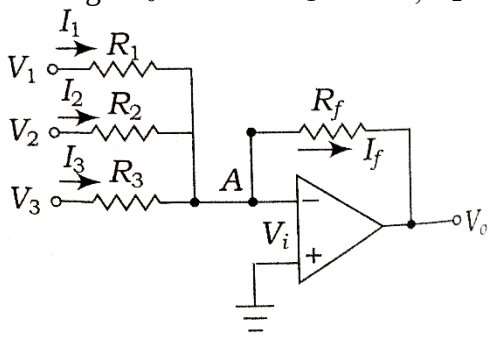
6. Design and draw op-amp based circuit for following operation:



7. Draw op-amp based circuit for following operation V_o = - (V_1+V_2+V_3)/3. Also state the value of input resistor if R_f=3kΩ. **[Ans: R_i = 9 kΩ]**
8. Design and draw the circuit for following operation using op-amp V_o=2V_1+V_2-5V_3
9. Draw and describe following op-amp based operation using log amplifier V_o=V_1×V_2
10. Suggest an OPAMP based circuit to perform below operation

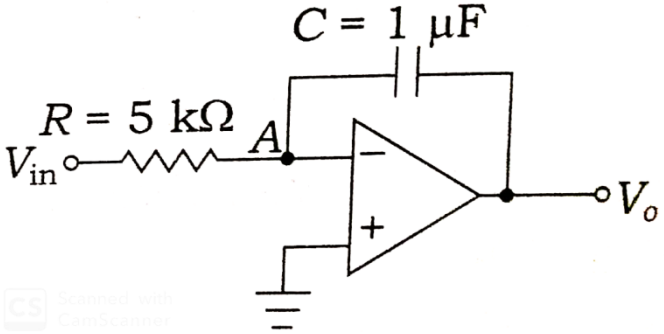


11. An op-amp is used as an inverting amplifier with a gain of 50. The input voltage is sinusoidal with maximum amplitude of 25 mV. What is the maximum frequency of the input voltage? Given slew rate is 0.5 V/μs. **[Ans: 63.694 kHz]**
12. An op-amp has a slew rate of 0.45 V/μs. How much time will it take to change the output voltage from 0V to 10 V? **[Ans: 22.23 μs]**
13. An adder circuit is shown in figure with V_1 = 1V, V_2 = 2V and V_3 = -2V. Determine the output voltage V_0. Assume R_1 = 2 kΩ, R_2 = 1 kΩ, R_3 = 2 kΩ and R_f = 4.7 kΩ.

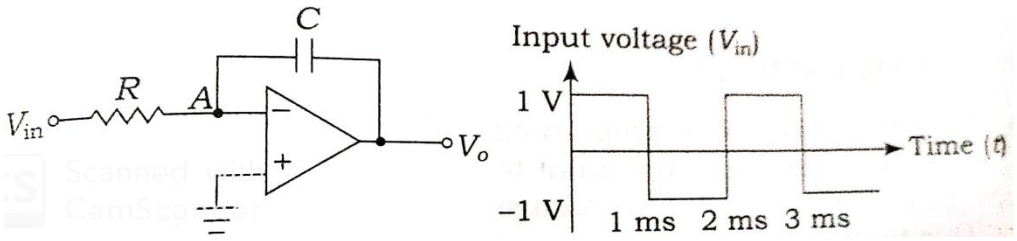


[Ans: -7.05 V]

14. An integrator circuit is shown in figure below. Find out the output voltage when the input voltage is $2sin\,1000\pi t$ and show the output voltage waveform. [Ans: $0.1273cos\,1000\pi t$]



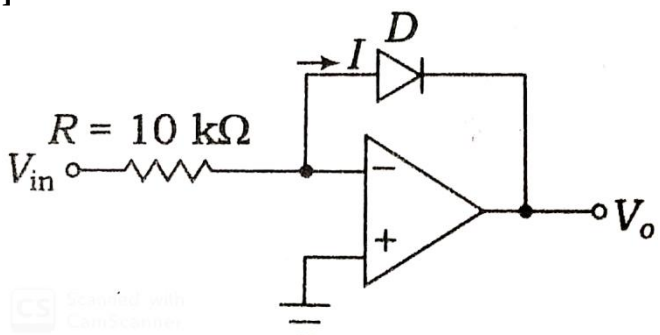
15. If a square wave is applied as input voltage to an integrator circuit as shown in figure below, find out the output voltage. Assume RC = 0.1 second. **[Ans: -10 mV, 0 V]**



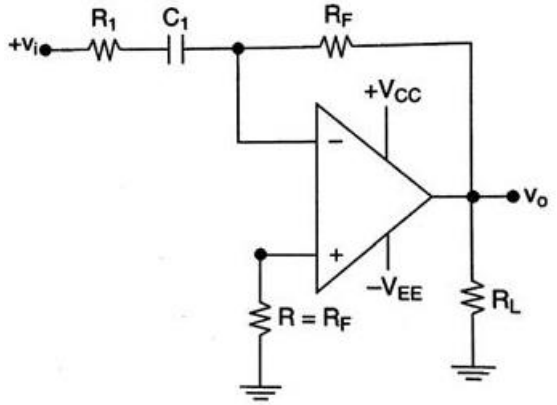
16. A log amplifier using an op-amp and diode is shown in figure given below. The characteristics of diode is expressed as

$$I = I_s\left(e^{\frac{qV_D}{KT}} - 1\right)$$

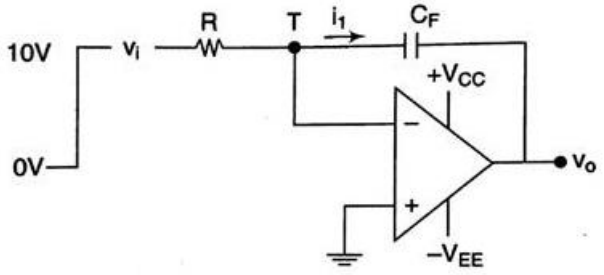
(a) Determine the output voltage in terms of input voltage V_{in}.
(b) Calculate the output voltage when KT/q = 20 mV, R = 10 kΩ and I_s = 1 μA. **[Ans: 73.77 mV]**



17. Determine the value of R_1, R_F and C_1 in the practical differentiator of the form shown below to satisfy the specifications: -Differentiator break frequency f_c = 2 kHz and maximum closed loop gain A_F = 5. **[Ans: R_1 = 796 Ω, R_F = 3.98 kΩ, C_1 = 0.1 μF]**



18. In the following integrator circuit used to generate voltage ramps, if R=5 kΩ, C=1μF and input is a step voltage of +10V, at what rate does the output voltage change? **[Ans: 2 V/ms]**



19. Draw a practical integrator that integrates signal with frequencies down to 200 Hz and produces a peak output of 0.2V when the input is 10V peak sine wave of frequency 10 kHz.

Conversion (D/A converter and R-2R ladder)

20. An 8 bit DAC has a resolution of 20mV/bit. What is the analog output voltage for the digital input code 00010110 (the MSB is the left most bit)? **[Ans: 0.42 V]**
21. For a 5-bit resistive divider, determine the following: (a) the weight assigned to the LSB; (b) the weight assigned to the second and third LSB; (c) the change in output voltage due to a change in the LSB, the second LSB, and the third LSB; (d) the output voltage for a digital input of 10101. Assume 0 = 0 V and 1 = + 10 V.
[Ans: (a) 1/31, (b) 4/31, (c) 10/31, 20/31, 40/31, (d) 6.77V]
22. What are the output voltages caused by each bit in a 5-bit ladder if the input levels are 0 = 0 V and 1 = +10 V? (a) Find the output voltage of this 5-bit ladder for digital input of 11010. (b) What is the full-scale output voltage.
[Ans: 5V, 2.5V, 1.25V, 0.625V, 0.3125V, (a) 8.125 V, (b) 9.6875 V]
23. What is the resolution of a 12-bit *D/*A converter which uses a binary ladder? If the full-scale output is + 10 V, what is the resolution in volts? **[Ans: 1/4096, 2.44 mV]**
24. What is the full-scale output voltage of a 6-bit binary ladder if 0 = 0 V and 1 = +10 V? Find the output voltage of a 6-bit binary ladder with the following inputs: (a) 101001, (b) 111011 and (c) 110001. **[Ans: 9.84375V,(a) 6.40625V,(b) 9.21875V,(c) 7.8125 V]**